Amendments to the Specification:

Please insert the following "Cross-Reference to Related Applications" section beginning at page 1, line 1:

This application is a continuation patent application of U.S. Patent Application No. 10/074,419, filed February 12, 2002, now U.S. Patent No. 6,694,347 and entitled "Switching Method in a Multi-Threaded Processor"; which is a divisional patent application of U.S. Patent Application No. 09/309,735, filed May 11, 1999, now U.S. Patent No. 6,507,862; the disclosures of which are hereby incorporated herein in their entireties.

This application is also related in subject matter to the following patent applications:

1. U.S. Patent Application No. 09/309,732, filed May 11, 1999, now U.S. Patent No. 6,938,147 and entitled "Processor with Multiple-Thread, Vertically-Threaded Pipeline".

2. U.S. Patent Application No. 09/309,731, filed May 11, 1999, now U.S. Patent No. 6,351,808 and entitled "Vertically and Horizontally Threaded Processor with Multidimensional Storage for Storing Thread Data".

3. U.S. Patent Application No. 09/309,730, filed May 11, 1999, now abandoned and entitled "Vertically-Threaded Processor by Multiple-Bit Flip-Flop Global Substitution".

4. U.S. Patent Application No. 09/309,734, filed May 11, 1999, now U.S. Patent No. 6,542,991 and entitled "Multiple-Thread Processor with Single-Thread Interface Shared Among Threads".

5. U.S. Patent Application No. 09/309,733, filed May 11, 1999, now U.S. Patent No. 6,341,347 and entitled "Thread Switch Logic in Multiple-Thread Processor".

Please replace the paragraph beginning at page 8, line 12, with the following paragraph, marked to show changes:

~~**FIGURE 16,**~~ **FIGURES 16A and 16B** are a schematic circuit diagram illustrates a suitable bit storage circuit storing one bit of the local registers for the multi-dimensional register file with eight windows.

Please replace the paragraph beginning at page 8, line 17, with the following paragraph, marked to show changes:

~~**FIGURE 18**~~ **FIGURES 18A-18D** is a schematic circuit diagram illustrating an implementation of a multi-dimensional register file for registers shared across a plurality of windows.

Please replace the paragraph beginning at page 34, line 18, with the following paragraph, marked to show changes:

The external cache control unit 1022 is also connected to a peripheral component interconnect (PCI) bus 1032 via a PCI controller 1030. The external cache control unit 1022 is further connected to a Dynamic Random Access Memory (DRAM) 1034 and an UltraPort Architecture Interconnect (UPA) bus 1026 via a memory control unit (MCU) 1028. The external cache control unit 1022 and the memory control unit (MCU) 1028 are unified between thread 0 and thread 1 to perform functions of cache miss processing and interfacing with external devices to supply, in combination, a plurality of execution threads to the thread 0 machine state block 1010 and the thread 1 machine state block 1012. The unified external cache control unit 1022 and memory control unit (MCU) 1028 include thread identifier (TID) tagging to specify and identify the thread that is accessed via the L2 cache SRAM 1024, the PCI bus 1032, the DRAM 1034, and the UPA bus 1026. The PCI controller 1030 and the MCU 1028 are shared between threads using a single port identifier. Thread ID tagging is implemented in processor components that are non-stalling including, for example, a carry (logN)-bit TID in L1 and L2 caches (both data and instruction caches), translation look-aside buffers (TLBs), asynchronous interfaces of load buffers, an external memory management unit (MMU) interface, and the like. In non-stalling components, only a single thread passes through the component at one time so that no stalled state exists that would be stored. The thread ID bits identify which thread is active in the component.